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A Digital-to-RF Converter Architecture Suitable for a Digital-to-RF Direct-Conversion Software Defined Radio Transmitter

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SUMMARY An architecture for a digital-to-RF converter for a software defined radio (SDR) transmitter is proposed The ideal hardware architecture for an SDR is a digital-signal to RF-signal direct conversion transmitter. However no conventional digital-to-analog converter (DAC) has converted over 1-GHz RF signal with enough resolution, in the present condition. In this paper, a digital-to-RF direct converter architecture using a $\Delta\Sigma$ modulation technique is proposed for the amplitude-phase modulated signal The experimental results show that the proposed direct converter outputs a sufficiently accurate signal.

key words: DAC, digital-to-RF direct-conversion, software defined radio, $\Delta\Sigma$ modulation

1. Introduction

A microprocessor operating with a clock frequency of 1 GHz was presented at the 1998 IEEE International Solid-state Circuit Conference (ISSCC98) [1] It implies that digital circuits can treat signals of a few hundred MHz and may be used as intermediate frequency (IF) signal processing stages in a cellular phone, instead of traditional analog IF stages. In the very near future, it is anticipated that clock frequencies may increase up to several GHz, and RF signals of a few GHz may be processed with a digital circuit.

However, no transceiver using digital intermediate frequency stages currently exists, because it would require very high-speed and high-resolution analog-to-digital/digital-to-analog converters (ADC/DAC) and they are not available to date.

In a conventional transmitter, lowpass filters are indispensable for suppressing undesired signals from the DAC; i e., quantization noise in adjacent channels and aliasing signals. In addition, an upconverter requires a bandpass filter to suppress a leaked local oscillation signal and an image signal. These filters limit flexibility of the transmitter. If a digital IF/RF stage is realized, the filtering functions are produced with digital circuits and digital circuits are more flexible than analog circuits. Digital circuits and digital signal processing already have potential to realize required functions but ADCs and DACs do not.

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In this paper, a digital-to-RF direct-converter architecture which converts the digital In-phase and Quadrature-phase (I/Q) modulation signals into the analog amplitude-phase modulated RF signal. It is obvious that this converter is a DAC, and this converter can be thought of as an SDR transmitter, because the conversion from I/Q modulation signals into modulated RF signal is the principal function of a transmitter. If the digital-to-RF direct converter is realized, an RF-to-digital direct converter will also be achieved, because a feedback loop containing a digital signal predictor, digital-to-RF converter, and error detector can operate as an RF-to-digital converter [2]. Therefore the digital-to-RF converter is the most critical component for realizing a digital-to-RF direct conversion software defined radio (SDR).

In the next section, we discuss design issues for a conventional-type high-speed and high-resolution DAC, and present our strategy for dealing with the issues. In Sect 3, the proposed architecture is described. Finally, experimental results and conclusions are presented.

2. Issues Concerning DACs in RF Stage

2.1 Frequency Response

In a radio communication system, DACs and amplifiers are required to have flat frequency characteristics. This flatness requirement makes designing high-speed DACs difficult.

Assuming the Thévenin equivalent circuit [3] of the DAC as shown in Fig 1, the frequency response of the DAC is

$$F(s) = \frac{1}{1 + sCR} \tag{1}$$

In this case, to realize 8-bit resolution from dc to 1 GHz, for example, the amplitude error of the DAC should be less than 1/2 LSB at 1 GHz, i e

$$\left| \frac{1}{1 + 1 \times 10^9 \times 2j\pi CR} \right| > 1 - \frac{1}{2}2^{-8} \tag{2}$$

This equation can be approximated and simplified as follows

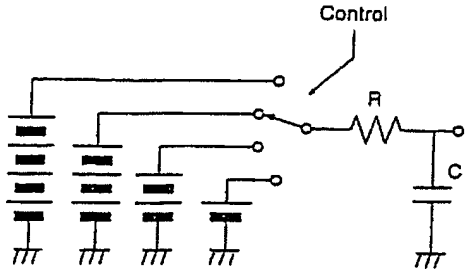

Fig. 1 Equivalent circuit of DAC.

$$|1 + 2 \times 10^9 j\pi CR| < 1 + 2^{-9}$$

$$1 + (2\pi \times 10^9 CR)^2 < 1 + 2 \times 2^{-9}$$

$$(2\pi \times 10^9 CR)^2 < 2^{-8}$$

$$CR < \frac{2^{-4}}{2\pi \times 10^9} \quad (3)$$

The bandwidth of this type of circuit is usually defined at 3-dB gain decreasing frequency. In the case of Eq. (1), the −3-dB frequency is,

$$f_{-3\mathrm{dB}} = \frac{1}{2\pi CR}. \quad (4)$$

Substituting Eq. (3) for Eq. (4), the −3-dB cut-off frequency of the DAC must exceed $2^4 = 16$ GHz. With silicon CMOS technology, it is impossible to realize the −3-dB frequency of 16 GHz.

Fortunately, RF front-end circuits are only required to have a flat frequency characteristic within a limited frequency band in which the radio communication system is allocated, and most RF circuits have essentially bandpass characteristics. This means that it is necessary for an SDR just to consider a bandpass-type DAC instead of a conventional lowpass-type DAC. The bandpass-type DAC, which is proposed in Sect. 3, is easier to realize than the lowpass type.

2.2 Non-Linearity

Non-linearity is another issue in designing a high-speed and high-resolution DAC For a low-frequency analog circuit, linearization techniques have been developed and they make non-linearity of transistors negligible by compensating for resistive non-linearity [4] However, for a high-frequency DAC, dynamic non-linearity caused by non-linear capacitors is more important, because non-linearity tends to degrade signal quality, and this tendency is particularly marked in the case of non-linearity of parasitic capacitances

For example, an MOS switch on a semiconductor chip has drain-substrate junction capacitance, which depends on the voltage between the drain and the substrate. Therefore, if a DAC contains MOS switches, the small-signal frequency-response will depend on the signal amplitude. To improve such a non-linearity, in this case, there are two ways. One is to make the frequency characteristic flat which can be achieved by letting the internal node impedance be low However, a lower node impedance makes the ratio of currents through the parasitic capacitors and resistive load small, and so this technique has the disadvantage of large current consumption.

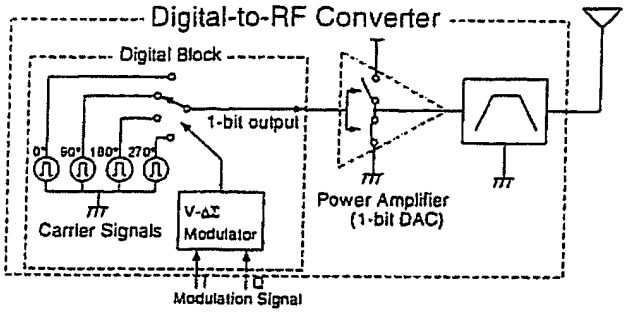

Fig. 2 Proposed architecture of the digital-to-RF direct converter.

The other way to improve non-linearity is to use a constant amplitude signal. Although it may seem strange for an SDR which treats amplitude modulated signals, there are some techniques for making an amplitude varying signal from constant amplitude pulses We introduce such a technique in the next section.

3. Proposed Architecture

3.1 Amplitude Modulated Signal from a 1-Bit DAC

Figure 2 shows our goal; the digital-to-RF direct converter which converts the digital In-phase and Quadrature-phase (I/Q) modulation signals into the analog amplitude-phase modulated RF signal. Each part of this converter is described in this section.

As mentioned in the previous section, there are some techniques for making an amplitude varying signal from constant amplitude pulses. For example, pulse width modulation (PWM), and pulse density modulation (PDM) are known as techniques which do this. They are used for high power-efficiency audio amplifiers. Figure 3(a) shows a simplified schematic of a class D amplifier. The switch is driven by an input pulse control signal of small power, and outputs a high-power pulse modulated signal. The output pulse modulated signal is demodulated by a lowpass filter The output signal $V_{out}(\omega)$ is given by the following equation:

$$V_{out}(\omega) = F_{\mathrm{LPF}}(\omega) V_{dc} P_a(\omega), \quad (5)$$

where $F_{\mathrm{LPF}}(\omega)$ is the frequency response of the lowpass filter, V_{dc} is the dc power supply voltage, and $P_a(\omega)$ is the normalized (1 or 0) input pulse control signal.

It is straightforward to generalize the class D amplifier into an amplitude modulator, as shown in

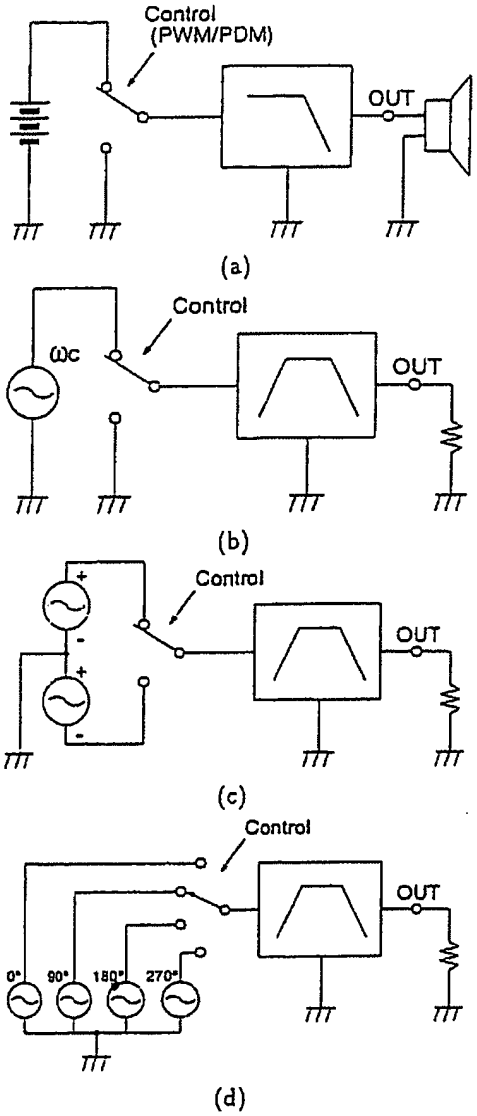

Fig. 3 (a) Class D audio amplifier, (b) Amplitude modulator, (c) Balanced modulator, (d) Quadrature modulator.

Fig. 3(b) The DC power source is replaced by a carrier signal source, and the lowpass filter is replaced by a bandpass filter (BPF) with a center frequency at the carrier frequency. The output signal $V_{out}(\omega)$ for this case is given by the following equation:

$$V_{out}(\omega) = F_{BPF}(\omega)\int_{-\infty}^{\infty} V_c(x)P_a(\omega - x)dx$$
$$= F_{BPF}(\omega)\sum_{n=-\infty}^{\infty} V_n P_a(\omega - \omega_n), \quad (6)$$

where $F_{BPF}(\omega)$ is the frequency response of the BPF, $V_c(\omega)$ is the carrier signal, and V_n is an amplitude of the n-th order harmonics of the carrier signal. Hereafter, we treat only the term $n = 1$ to simplify the discussion. If the clock frequency of the pulse modulation signal $P_a(\omega)$ and the carrier frequency are synchronized, the terms $n \neq 1$ are sufficiently small around the carrier frequency, and our desired signal is contained in $V_1 P_a(\omega - \omega_c)$.

The switching amplitude modulator can be extended as shown in Figs. 3(c) and (d). Figure 3(c) is a balanced modulator, and (d) is a quadrature modulator that consists of switches, respectively. The output of the quadrature modulator $V_{out}(\omega)$ is

$$V_{out}(\omega) = F_{BPF}(\omega)V_1 \{P_a(\omega - \omega_c) - P_b(\omega - \omega_c) + jP_c(\omega - \omega_c) - jP_d(\omega - \omega_c)\}$$
$$= F_{BPF}(\omega)V_1 P(\omega - \omega_c), \quad (7)$$

where $P_a(\omega), P_b(\omega), P_c(\omega)$, and $P_d(\omega)$ are spectra of pulse streams, and $P(\omega) = \{P_a(\omega) - P_b(\omega)\} + j\{P_c(\omega) - P_d(\omega)\}$. In the time domain, only one term of P_x $(x = a, b, c, d)$ is 1 and the others are 0 for any instant, and P results in 1, or -1, or j, or $-j$. Consequently, an amplitude-phase modulated signal is generated by using switches and a BPF. This modulator is free from the non-linearity of transistors, because the input and output signal of switching transistors consist of constant amplitude pulse streams.

3.2 Noise Shaping

There is the following issue respecting the pulse modulation technique for digital-to-RF direct converters: the resolution of a DAC using pulse modulation seems to be low because the pulse signal is only 1 bit. This issue has been studied in terms of quantization noise of a pulse modulated signal, and it is known that the $\Delta\Sigma$ modulation has a big advantage. The quantization noise spectrum of a $\Delta\Sigma$ modulated signal can be 'shaped', and the quantization noise in a desired frequency band can be suppressed.

Figure 4(a) shows a basic $\Delta\Sigma$ modulator [5], [6]. The feedback loop makes the difference between input and output signal small when the loop gain is sufficiently high. The integrator makes the loop gain at 0 Hz (dc) infinity. As a result, the difference between the input and output signal, which is called quantization noise, is small at low frequency and large at high frequency.

A generalized version of the conventional $\Delta\Sigma$ modulator is shown in Fig. 4(b). The integrator may be replaced by higher-order filters (linear system), and the comparator is replaced by a low-resolution multibit ADC and outputs a multibit over-sampled signal.

Figure 4(c) shows a proposed vector $\Delta\Sigma$ modulator [10]. It is a vector extension of the conventional $\Delta\Sigma$ modulation for In-phase and Quadrature-phase vector modulation. A modulation signal $X(z^{-1}) = [x_I(z^{-1}), x_Q(z^{-1})]^t$ and a feedback signal $Y(z^{-1}) = [y_I(z^{-1}), y_Q(z^{-1})]^t$ are fed to the linear system. The

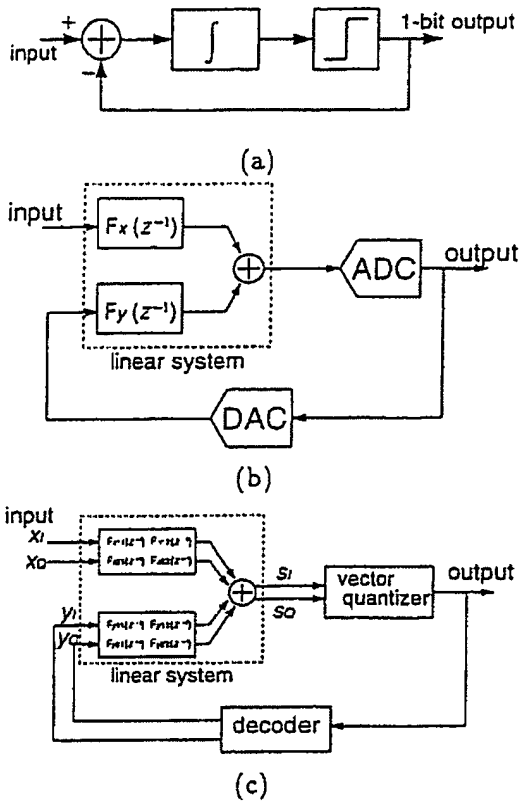

Fig. 4 (a) Block diagram of a basic $\Delta\Sigma$ modulator (b) Generalized $\Delta\Sigma$ modulator (c) Vector $\Delta\Sigma$ modulator

output signal of the linear system is

$$S(z^{-1}) = \left[s_I(z^{-1}), s_Q(z^{-1})\right]^t = F_x(z^{-1})X(z^{-1}) + F_y(z^{-1})Y(z^{-1}) \quad (8)$$

where $F_x(z^{-1})$ and $F_y(z^{-1})$ are 2×2 matrices whose elements are linear transfer functions.

To drive our switching quadrature modulator, a vector quantizer maps the input vector $S(z^{-1}) = \left[s_I(z^{-1}), s_Q(z^{-1})\right]^t$ into alphabetic code A, B, C, and D by a rule, as shown in Fig 5. When the input vector $[s_I(z^{-1}), s_Q(z^{-1})]^t$ is in region A, the vector quantizer outputs code A, and the code A represents $1+0j$. Likewise, the input vector in regions B, C, and D are mapped to code B, C, and D which represent $-1+0j$, $0+j$, and $0-j$, respectively The output code is obtained as the pulse stream $P = \{P_a - P_b\} + j\{P_c - P_d\}$, as mentioned in the previous section

The decoder decodes the code stream and outputs $[1,0]^t$, or $[-1,0]^t$, or $[0,1]^t$, or $[0,-1]^t$ as the feedback vector $Y(z^{-1})$. Note that the feedback vector Y, the output alphabetic code of the vector $\Delta\Sigma$ modulator, and the pulse modulation signal $P(\omega)$ are different expressions of an identical signal.

The relation between $S(z^{-1})$ and $Y(z^{-1})$ is

$$Y(z^{-1}) = S(z^{-1}) + E(z^{-1}), \quad (9)$$

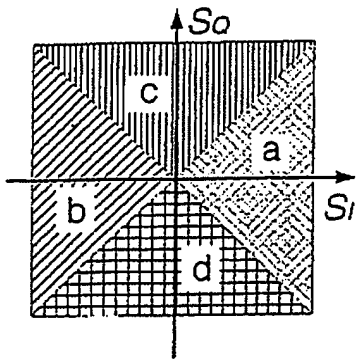

Fig. 5 Mapping from input vector into alphabetic code.

where $E(z^{-1})$ is the quantization noise. By eliminating $S(z^{-1})$ from Eqs. (8) and (9), we have an equation that describes the operation of a vector $\Delta\Sigma$ modulator: i.e.

$$\begin{aligned} Y(z^{-1}) &= \left[I - F_y(z^{-1})\right]^{-1} \\ &\quad \left[F_x(z^{-1})X(z^{-1}) + E(z^{-1})\right] \\ &= F_{st}(z^{-1})X(z^{-1}) \\ &\quad + F_{ns}(z^{-1})E(z^{-1}), \end{aligned} \quad (10)$$

where I is the unit matrix. $F_{st}(z^{-1})$ and $F_{ns}(z^{-1})$ are called the signal transfer function and the noise shaping function, respectively.

When ω_s is the sampling clock frequency of the vector $\Delta\Sigma$ modulator, the relation between z and ω is $z = e^{2\pi j \frac{\omega}{\omega_s}}$. The spectrum of the pulse modulated signal $P(\omega)$ is given by

$$\begin{aligned} P(\omega) &= y_I(z^{-1}) + jy_Q(z^{-1}) \\ &= [1, j]\, Y(z^{-1}) \\ &= [1, j]\, Y(e^{-2\pi j \frac{\omega}{\omega_s}}) \\ &= [1, j]\, \{F_{st}(e^{-2\pi j \frac{\omega}{\omega_s}})X(e^{-2\pi j \frac{\omega}{\omega_s}}) \\ &\quad + F_{ns}(e^{-2\pi j \frac{\omega}{\omega_s}})E(e^{-2\pi j \frac{\omega}{\omega_s}})\}. \end{aligned} \quad (11)$$

Substituting Eq. (11) for Eq. (7), the desired output of the proposed modulator $D(\omega)$ is given by

$$\begin{aligned} D(\omega) &= F_{\mathrm{BPF}}(\omega)V_1 \\ &\quad [1, j]\, F_{st}(e^{-2\pi j \frac{\omega-\omega_c}{\omega_s}})X(e^{-2\pi j \frac{\omega-\omega_c}{\omega_s}}), \end{aligned} \quad (12)$$

and the undesired output $U(\omega)$ is

$$\begin{aligned} U(\omega) &= F_{\mathrm{BPF}}(\omega)V_1 \\ &\quad [1, j]\, F_{ns}(e^{-2\pi j \frac{\omega-\omega_c}{\omega_s}})E(e^{-2\pi j \frac{\omega-\omega_c}{\omega_s}}). \end{aligned} \quad (13)$$

The vector $\Delta\Sigma$ modulator and the 1-bit quadrature modulator are realized in the digital block as shown in Fig 2. The output signal of the digital block is 1 bit and drives a switching power amplifier as a 1-bit DAC If the system is successfully designed, the noise shaping function suppresses undesired signals in the passband of the bandpass filter. The resultant noise

level is equivalent to a multibit high-resolution DAC in the passband. This system is a bandpass DAC and suitable for digital-to-RF direct conversion SDR transmitter

4. Experimental Results

Figure 6 shows the experimental setup to confirm the function of the proposed vector $\Delta\Sigma$ modulator. The vector $\Delta\Sigma$ modulator, and the 1-bit quadrature modulator are implemented using a C language program on a PC. The output pulse stream is stored in the memory of the arbitrary waveform generator (AWG), which is used as a memory bank. A 100-MHz clock signal is input to the AWG and a 1-bit 100-Ms/s signal is obtained. Figure 7 shows the measured AWG output signal spectrum when the I and Q modulation signals are sinusoidal signals in quadrature to obtain the image rejection output. The Y-axis is normalized by the desired sideband magnitude.

This result has a residual undesired image signal at 24.756 MHz, which is due to calculation error. A 244-kHz signal sampled at 100 Ms/s can make a $0.5 \times 360 \times 0.244/100 \simeq 0.44$ degree phase error, which corresponds to the image rejection ratio of -42 dBc. It agrees with the measured result shown in Fig. 7. This phase error can be compensated for by software modification.

Equation (12) shows that the modulation signal $X(z^{-1})$ is linearly transformed into the desired output signal $D(\omega)$. However, there is a limitation because the desired signal power cannot exceed the output pulse signal power Figure 7 is the result when the desired signal amplitude is 0.6 of the pulse amplitude

The quantization noise is observed to be shaped by the noise shaping function $F_{ns}(z^{-1})$ and the noise spectrum has a notch at 25 MHz, because the $F_{ns}(z^{-1})$ is designed to have a 2nd order zero at the center frequency The noise level seems to depend on the desired signal amplitude because the amplitude of the output pulse stream is constant, and the pulse stream consists of the desired signal and the quantization noise. However, the noise power in signal band is often estimated as it is independent of desired signal power, and it is known that the estimation agrees with experimental result [6].

To obtain a high-frequency amplitude-phase modulated signal, we used a 1-bit upconverter fabricated in 0.25-μm silicon CMOS technology. Figure 8 shows the experimental setup of a 1-GHz DAC. The upconverter consists of an exclusive-OR circuit and an output buffer. The output buffer acts as a 1-bit digital-to-analog converter, and the buffer corresponds to the power amplifier in Fig. 2.

Figure 9 shows the up-converted signal spectrum The desired signal of -6.5 dBm is obtained at a current dissipation of 33 mA from a 2.7-V power supply.

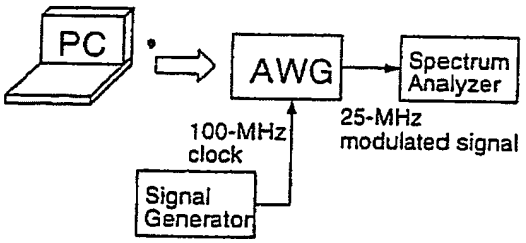

Fig. 6 Experimental setup.

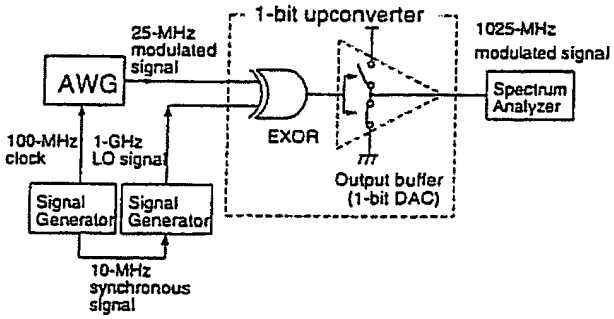

Fig. 8 Experimental setup of 1-GHz DAC

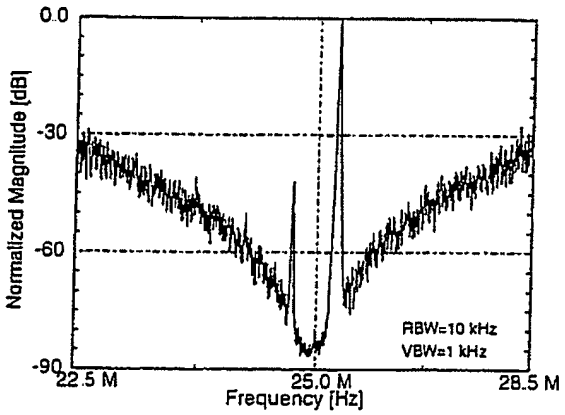

Fig. 7 AWG output signal spectrum

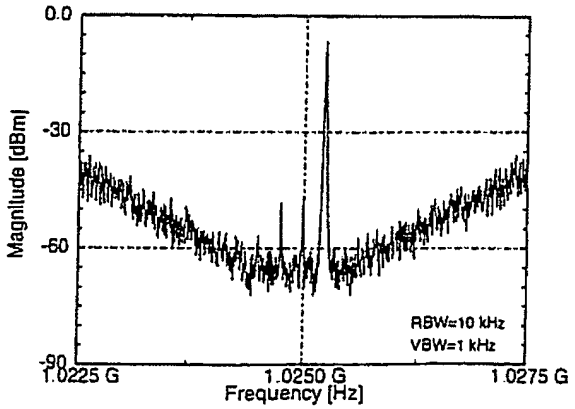

Fig. 9 Up-converter output signal spectrum

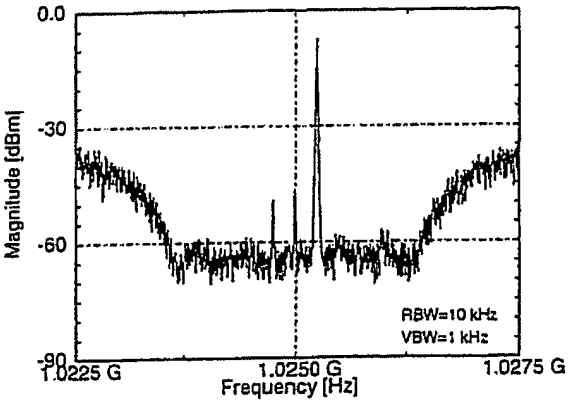

Fig. 10 Noise shaping with higher-order noise shaping function.

A shallower notch in the noise spectrum than in Fig. 7 is observed. This is supposed to be caused by the phase noise (jitter) of the local oscillation (LO) signal, and noise from the up-converter circuit. A carrier leak and an undesired sideband signal can be seen; however, they are at least 40 dB smaller than the desired signal. They are sufficiently small for cellular phone systems, because leakage from conventional analog quadrature modulators is the same level [7]–[9] Note that the leakage from a conventional transmitter is larger than that because I/Q DACs and I/Q baseband filters make I/Q signal error.

Consequently, this result is evidence that a 1-GHz amplitude phase modulated signal is obtained with a 0.25-μm silicon CMOS DAC.

Figure 10 shows the noise spectrum with 6th order noise shaping function $F_{ns}(z^{-1})$, when the modulation signal amplitude is 0.6 of the pulse amplitude. The noise shaping function has wide-band elimination characteristics. A noise-suppressed band is centered at 1025 MHz and has about 3-MHz bandwidth. It means that the requirement for the RF bandpass filter can be eased. In addition, this result indicates an advantage of the digital-to-RF direct-conversion system. The 3rd or 5th order distortion is very small. It means that the adjacent channel leakage power is small.

If a wider bandwidth is required, the sample rate must be raised in proportion to the required bandwidth. For example, when a 30-MHz bandwidth digital-to-RF converter is required, a 1-Gs/s 1-bit signal generator is needed

5. Conclusions

An architecture of a digital-to-RF direct converter is proposed, and experimental results show that the direct converter generates a sufficiently accurate signal at 1 GHz This converter has three advantages over conventional DACs: First, high speed is easy to achieve because of the simple 1-bit structure The upper frequency limit of proposed converter is the same as that of an inverter circuit Second, the class D output stage has possibility of realizing a high power efficiency. If the switching transistors and the RF bandpass filter are optimized, the power efficiency may be as high as that of a class E or class F amplifier Third, the adjacent channel power leakage is very low The low adjacent channel leakage is important for radio communication system design, because adjacent channel leakage limits the spectral efficiency.

However, there are some design issues concerning the reduction of power dissipation; such as deciding, which implementation of the vector $\Delta\Sigma$ modulation is better, hardware or software, and, how to share the noise suppression function between the RF bandpass filter and the noise shaping function. For more successful SDR development, co-design of the RF bandpass filter and the noise shaping function is required from now on.

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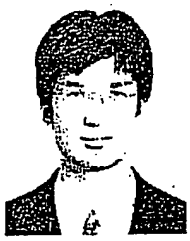

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